

09 "MK-10" Pamił mikrokomputera CAS.

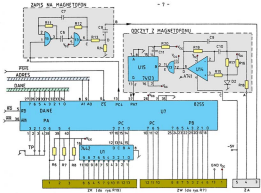
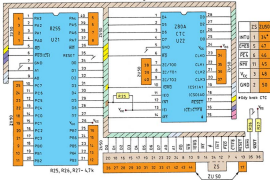
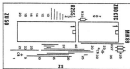


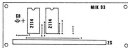
Рис. 1. Принципиальная схема порта ввода/вывода микрокомпьютера CA80.



RH "PIL" Study will also verify the presence of the photo verification.



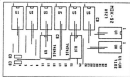
R12 Układ wejściowy układowiska.



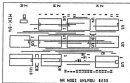
R13 Układ zastępczy panelu BAP (UGS).



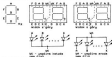
R18 Rozbudowa płytki MIC95.



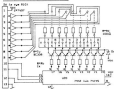
R13 Układ zastępczy panelu BAP (UGS).



R14 Układ zastępczy portu systemowego (BSPS).

[illegible]

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Figure 1 consists of two histograms. The left histogram is titled 'Histogram of the number of correct answers for the 100-item test'. The x-axis is labeled 'Number of correct answers' and ranges from 0 to 100. The y-axis is labeled 'Frequency' and ranges from 0 to 10. The distribution is right-skewed, with a peak at 0 correct answers. The right histogram is titled 'Histogram of the number of correct answers for the 100-item test with a 10-item bonus'. The x-axis is labeled 'Number of correct answers' and ranges from 0 to 110. The y-axis is labeled 'Frequency' and ranges from 0 to 10. The distribution is also right-skewed, with a peak at 0 correct answers.

JUMP	DATA	RETURN	REGISTER	REGISTER	STATUS (bits)	ACCUMULATOR*	ACCUMULATOR*
00 JP 00, 00	00 CALL 00, 00	00 RET	CALL	00 RLO	00 10 0, 0	00 ACC A, B	00 00 0
01 JP 00, 00	01 CALL 00, 00	01 RET 00	CP RST 000	01 RRO	01 10 0, 0	01 ACC A, C	01 00 0
02 JP 00, 00	02 CALL 00, 00	02 RET 00	CP RST 000	10 RLA	02 10 0, 0	02 ACC A, D	02 00 0
03 JP 00, 00	03 CALL 00, 00	03 RET 00	CP RST 000	11 RRA	03 10 0, 0	03 ACC A, E	03 00 0
04 JP 00, 00	04 CALL 00, 00	04 RET 00	CP RST 000	12 RLC	04 10 0, 0	04 ACC A, F	04 00 0
05 JP 00, 00	05 CALL 00, 00	05 RET 00	CP RST 000	13 RRC	05 10 0, 0	05 ACC A, G	05 00 0
06 JP 00, 00	06 CALL 00, 00	06 RET 00	CP RST 000	14 RLC	06 10 0, 0	06 ACC A, H	06 00 0
07 JP 00, 00	07 CALL 00, 00	07 RET 00	CP RST 000	15 RRC	07 10 0, 0	07 ACC A, I	07 00 0
08 JP 00, 00	08 CALL 00, 00	08 RET 00	CP RST 000	16 RLC	08 10 0, 0	08 ACC A, J	08 00 0
09 JP 00, 00	09 CALL 00, 00	09 RET 00	CP RST 000	17 RRC	09 10 0, 0	09 ACC A, K	09 00 0
10 JP 00, 00	10 CALL 00, 00	10 RET 00	CP RST 000	18 RLC	10 10 0, 0	10 ACC A, L	10 00 0
11 JP 00, 00	11 CALL 00, 00	11 RET 00	CP RST 000	19 RRC	11 10 0, 0	11 ACC A, M	11 00 0
12 JP 00, 00	12 CALL 00, 00	12 RET 00	CP RST 000	20 RLC	12 10 0, 0	12 ACC A, N	12 00 0
13 JP 00, 00	13 CALL 00, 00	13 RET 00	CP RST 000	21 RRC	13 10 0, 0	13 ACC A, O	13 00 0
14 JP 00, 00	14 CALL 00, 00	14 RET 00	CP RST 000	22 RLC	14 10 0, 0	14 ACC A, P	14 00 0
15 JP 00, 00	15 CALL 00, 00	15 RET 00	CP RST 000	23 RRC	15 10 0, 0	15 ACC A, Q	15 00 0
16 JP 00, 00	16 CALL 00, 00	16 RET 00	CP RST 000	24 RLC	16 10 0, 0	16 ACC A, R	16 00 0
17 JP 00, 00	17 CALL 00, 00	17 RET 00	CP RST 000	25 RRC	17 10 0, 0	17 ACC A, S	17 00 0
18 JP 00, 00	18 CALL 00, 00	18 RET 00	CP RST 000	26 RLC	18 10 0, 0	18 ACC A, T	18 00 0
19 JP 00, 00	19 CALL 00, 00	19 RET 00	CP RST 000	27 RRC	19 10 0, 0	19 ACC A, U	19 00 0
20 JP 00, 00	20 CALL 00, 00	20 RET 00	CP RST 000	28 RLC	20 10 0, 0	20 ACC A, V	20 00 0
21 JP 00, 00	21 CALL 00, 00	21 RET 00	CP RST 000	29 RRC	21 10 0, 0	21 ACC A, W	21 00 0
22 JP 00, 00	22 CALL 00, 00	22 RET 00	CP RST 000	30 RLC	22 10 0, 0	22 ACC A, X	22 00 0
23 JP 00, 00	23 CALL 00, 00	23 RET 00	CP RST 000	31 RRC	23 10 0, 0	23 ACC A, Y	23 00 0
24 JP 00, 00	24 CALL 00, 00	24 RET 00	CP RST 000	32 RLC	24 10 0, 0	24 ACC A, Z	24 00 0
25 JP 00, 00	25 CALL 00, 00	25 RET 00	CP RST 000	33 RRC	25 10 0, 0	25 ACC A, [HL]	25 00 0
26 JP 00, 00	26 CALL 00, 00	26 RET 00	CP RST 000	34 RLC	26 10 0, 0	26 ACC A, [HL]	26 00 0
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28 JP 00, 00	28 CALL 00, 00	28 RET 00	CP RST 000	36 RLC	28 10 0, 0	28 ACC A, [HL]	28 00 0
29 JP 00, 00	29 CALL 00, 00	29 RET 00	CP RST 000	37 RRC	29 10 0, 0	29 ACC A, [HL]	29 00 0
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40 JP 00, 00	40 CALL 00, 00	40 RET 00	CP RST 000	48 RLC	40 10 0, 0	40 ACC A, [HL]	40 00 0
41 JP 00, 00	41 CALL 00, 00	41 RET 00	CP RST 000	49 RRC	41 10 0, 0	41 ACC A, [HL]	41 00 0
42 JP 00, 00	42 CALL 00, 00	42 RET 00	CP RST 000	50 RLC	42 10 0, 0	42 ACC A, [HL]	42 00 0
43 JP 00, 00	43 CALL 00, 00	43 RET 00	CP RST 000	51 RRC	43 10 0, 0	43 ACC A, [HL]	43 00 0
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45 JP 00, 00	45 CALL 00, 00	45 RET 00	CP RST 000	53 RRC	45 10 0, 0	45 ACC A, [HL]	45 00 0
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48 JP 00, 00	48 CALL 00, 00	48 RET 00	CP RST 000	56 RLC	48 10 0, 0	48 ACC A, [HL]	48 00 0
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51 JP 00, 00	51 CALL 00, 00	51 RET 00	CP RST 000	59 RRC	51 10 0, 0	51 ACC A, [HL]	51 00 0
52 JP 00, 00	52 CALL 00, 00	52 RET 00	CP RST 000	60 RLC	52 10 0, 0	52 ACC A, [HL]	52 00 0
53 JP 00, 00	53 CALL 00, 00	53 RET 00	CP RST 000	61 RRC	53 10 0, 0	53 ACC A, [HL]	53 00 0
54 JP 00, 00	54 CALL 00, 00	54 RET 00	CP RST 000	62 RLC	54 10 0, 0	54 ACC A, [HL]	54 00 0
55 JP 00, 00	55 CALL 00, 00	55 RET 00	CP RST 000	63 RRC	55 10 0, 0	55 ACC A, [HL]	55 00 0
56 JP 00, 00	56 CALL 00, 00	56 RET 00	CP RST 000	64 RLC	56 10 0, 0	56 ACC A, [HL]	56 00 0
57 JP 00, 00	57 CALL 00, 00	57 RET 00	CP RST 000	65 RRC	57 10 0, 0	57 ACC A, [HL]	57 00 0
58 JP 00, 00	58 CALL 00, 00	58 RET 00	CP RST 000	66 RLC	58 10 0, 0	58 ACC A, [HL]	58 00 0
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62 JP 00, 00	62 CALL 00, 00	62 RET 00	CP RST 000	70 RLC	62 10 0, 0	62 ACC A, [HL]	62 00 0
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94 JP 00, 00	94 CALL 00, 00	94 RET 00	CP RST 000	102 RLC	94 10 0, 0	94 ACC A, [HL]	94 00 0
95 JP 00, 00	95 CALL 00, 00	95 RET 00	CP RST 000	103 RRC	95 10 0, 0	95 ACC A, [HL]	95 00 0
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98 JP 00, 00	98 CALL 00, 00	98 RET 00	CP RST 000	106 RLC	98 10 0, 0	98 ACC A, [HL]	98 00 0
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114 JP 00, 00	114 CALL						

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TP

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