Technical Note

SoundPort™ Codecs

CODEC PCB AND CIRCUIT APPLICATION GUIDELINES

INTRODUCTION

Mixed signal grounding and bypassing, include the following brief notes and comments as a general "good-practice" guide for mixed signal printed circuit board design.

DECOUPLING AND BYPASSING

The power supply decoupling and bypassing is shown in Figure 1. It needs to be emphasized that low ESL 10nF to 100nF surface mount ceramic capacitors must be mounted right at the leads of the chip (or at least within a couple of mm). Remember the "rules-of-thumb" for trace length -- L ~ 1nH/mm, R ~ 2mOhm/mm (for common 10mil wide traces, 1oz foil).

POWER SUPPLIES

Avoid switch mode power supplies near ADC's, DAC's and analog circuits. Sometimes it is easier to use a separate 5V three terminal regulator, near the chip, for the analog supply. A 22uF tantalum or aluminum capacitor at the board edge helps to reduce power supply noise and the ESR damps ringing from decoupling chokes.

GROUND PLANE

ADI recommends extending the ground plane philosophy to include separate digital and analog power planes directly over their respective ground planes -- no overlapping of planes. The two plane pairs should be separated by a 2-3 mm gap. This means using a four layer board with the ground and power planes forming an internal, high capacitive, sandwich. This gives an extremely effective, low ESR & ESL bypass capacitor consisting of the separate ground and power planes themselves, with an effective capacitance of ~5pF/cm^2 (~30pF/in^2). The IC leads will have pads and vias that go directly to the appropriate plane for power and ground. All digital components are mounted over the digital power/ground plane sandwich and all analog components over the analog power/ground sandwich. This doesn't avoid the need for additional ceramic bypass capacitors at the IC pins as mentioned above. The importance and effectiveness of ground planes cannot be over emphasized, both to optimize the performance of the mixed signal part but also to reduce EMI.

LINKING GROUND PLANES

A single link between the two planes should be established, preferably close to the chip itself using a zero ohm resistor or ferrite bead. This is necessary to prevent any potential difference due to ESD or fault currents that could otherwise flow through the chip substrate with damaging affect but still isolate the planes to high frequency currents. It may be useful to provide for removable links in the prototype, at several locations, to permit debugging and testing for ground isolation. There should not be ANY digital or analog signal traces crossing the gap between the digital and analog planes.

DIGITAL SIGNALS AND COMPONENTS

All digital signals and components should be located away from analog circuitry. All high-speed digital traces should take the most direct route over the digital ground or power plane.

SOCKETS

Avoid the use of IC sockets.

PLD'S AND VLSI LOGIC CHIPS

Don't overlook adjacent PLD's and VLSI logic chips on the same PC board. These chips frequently include lots of synchronous logic and generate large switching currents that can infiltrate the rest of the board. Make sure they are well bypassed -- at the chip pins! This will not only ensure their reliable operation but reduce noise on the supply lines.

MULTIPLE CRYSTAL (CLOCK) OSCILLATORS

Be aware of problems that might occur due to multiple crystal (clock)oscillators, e.g. beats between harmonics that can enter the CODEC through either the analog or digital supplies or signal and voltage reference pins. If possible, enable only a single oscillator on a PC board at a

time or derive all the required frequencies from a single oscillator.

TRADITIONAL DESIGN PROBLEMS

Watch out for "traditional" design problems:

- Ground loop area (inductive coupling) - minimize loop area.
- Common impedance (current) coupling - minimize common impedance or use star points.
- Capacitive (voltage) coupling - separate, shield or lower circuit impedance.
- Surface and/or bulk leakage - separate, guard, conformal coat.
- Parallel trace coupling (combinations of above) - separate, terminate in characteristic impedance, use ground plane and/or intermediate grounded traces or use a slower logic family.

CAPACITIVE COUPLING

Watch out for capacitive coupling from the body of large components. Use the "outside foil ring", marked on capacitors, to identify which end to connect to ground.

MAGNETIC FIELDS

Watch out for the external magnetic field of inductors and transformers. Use electrostatic and magnetically shielded components if necessary. RF decoupling chokes can be mounted at right angles to minimize mutual inductance or try ferrite beads. Power transformers should be mounted off the board and oriented, with the most intense area of their external field, away from critical analog circuits. Use toroidal power transformers to reduce magnetic external fields.

CAPACITIVE LOADING

Minimize capacitive loading on digital output pins. For digital signals, driving 'long' traces, it may be necessary to terminate the trace in it's characteristic impedance to prevent over/undershoot and ringing. Z_0 is ÷80Ω for most applications and a series RC combination of 82Ω and 50pF will effectively terminate the end of a long trace in many cases.

INPUT SIGNAL EXCURSIONS

Ensure that offset biased, 5 volt CODEC/ADC analog input signals, can NOT go above Vcc or below ground even momentarily. Use low leakage diode 'clamps' or five volt single rail Op-Amps buffers to limit the input signal excursions.

EMI/RFI REQUIREMENTS

Consider EMI/RFI requirements for analog input and output lines. Input lines can radiate and receive RF and Sigma-Delta DAC outputs contain harmonic products from the de-sampling process up to 100MHz.

ASSUMPTIONS

Finally - remember when debugging, that every assumption is suspect!!

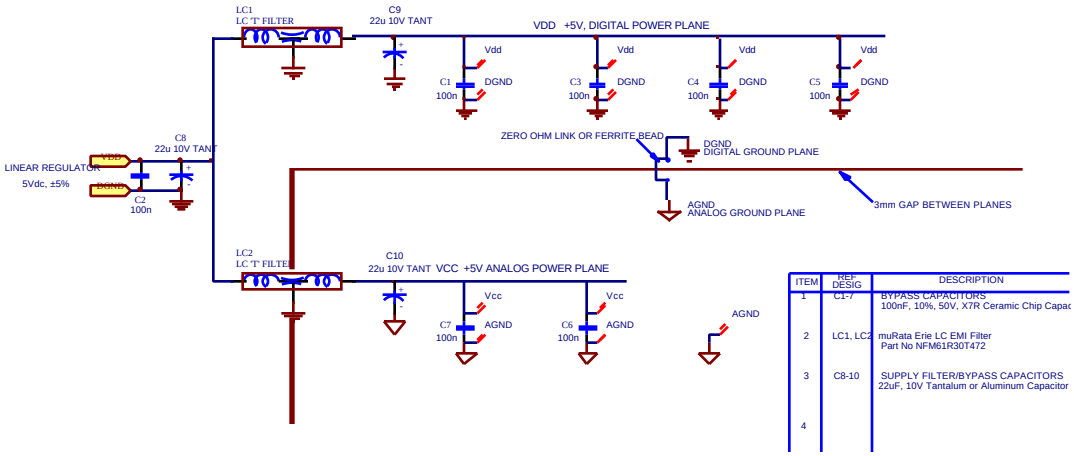

Figure 1. Mixed Signal Power, Grounding and Bypassing

REFERENCES

Additional, general high-speed and mixed-signal design, information is available in our seminar handbooks and application manuals as noted below. They are recommended as a source of good techniques and inspiration.

1. "Mixed Signal Processing Design Seminar", Analog Devices Inc., 1991, ISBN-0-916550-08-7
2. "High Speed Design Seminar", Analog Devices Inc., 1990, ISBN 0-916550-07-9
3. "Applications Reference Manual", Analog Devices Inc., 1993. Especially refer to collected Application Notes - Section 24, AN214, AN280, AN282, AN345, AN346, AN347, AN353, AN362.
4. "Noise Reduction Techniques in Electronic Systems, 2nd Ed", Henry W. Ott, Wiley Interscience, 1988.
5. "Interfacing Techniques in Digital Design With Emphasis on Microprocessors", Ronald L. Krutz, John Wiley, 1988.
6. "Audio/Video Reference Manual", Analog Devices Inc., 1992.
7. "Systems Application Guide", Analog Devices Inc., 1993, ISBN 0-916550-13-3
8. "High-Speed Digital Design, A Handbook of Black Magic", H.W. Johnson, M. Graham, PTR Prentice Hall, 1993. ISBN 0-13-395724-1